What is claimed is:

1.   A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

executing two one-dimensional inverse discrete cosine transforming functions, each of the functions being controlled to operate on a matrix of coefficients in either of two different directions.

2.   The method of claim 1 in which one of the directions is row order.

3.   The method of claim 1 in which one of the directions is column order.

4.   The method of claim 1 in which a sequencer determines which direction each function operates in for a given matrix.

5.   The method of claim 1 in which an address generator generates an address for each coefficient in the matrix.

6.   The method of claim 1 in which the functions are concurrently executed in the same direction on two different matrices of coefficients.

7.   The method of claim 1 in which the functions are concurrently executed in the same direction, the functions

3   switching periodically and concurrently to the other

4   direction.

1   8.   A storage medium bearing a machine-readable program

2   capable of causing a machine to:

3   execute two one-dimensional inverse discrete cosine

4   transforming functions, each of the functions being controlled

5   to operate on a matrix of coefficients in either of two

6   different directions.

1   9.   The medium of claim 8 in which one of the directions

2   is row order.

1   10.   The medium of claim 8 in which one of the directions

2   is column order.

1   11.   The medium of claim 8 in which a sequencer

2   determines which direction each function operates in for a

3   given matrix.

1   12.   The medium of claim 8 in which an address generator

2   generates an address for each coefficient in the matrix.

1   13.   The medium of claim 8 in which the functions are

2   concurrently executed in the same direction on two different

3   matrices of coefficients.

1   14.   The medium of claim 8 in which the functions are

2   concurrently executed in the same direction, the functions

3   switching periodically and concurrently to the other

4   direction.

1   15.   A method of implementing a two-dimensional inverse

2   discrete cosine transform, comprising:

3   executing a first one-dimensional inverse discrete cosine

4   transforming function in a first direction on a first matrix

5   of coefficients to produce a matrix of intermediate results;

6   and

7   executing a second one-dimensional inverse discrete

8   cosine transforming function in a second, different direction

9   on the matrix of intermediate results concurrent with the

10   first function executing in the second direction on a second

11   matrix of coefficients.

1   16.   The method of claim 15 in which the first direction

2   is row order.

1   17.   The method of claim 15 in which the first direction

2   is column order.

1   18.   The method of claim 15 in which the functions switch

2   periodically and concurrently between the first and second

3   directions.

1   19.   A storage medium bearing a machine-readable program

2   capable of causing a machine to:

3   execute a first one-dimensional inverse discrete cosine

4   transforming function, where the first function executes in a

5   first direction on a first matrix of coefficients, producing a

6   matrix of intermediate results; and

7   execute a second one-dimensional inverse discrete cosine

8   transforming function, where the second function executes in a

9   second, different direction on the matrix of intermediate

10   results concurrent with the first function executing in the

11   second direction on a second matrix of coefficients.

1   20.   The medium of claim 19 in which the first direction

2   is row order.

1   21.   The medium of claim 19 in which the first direction

2   is column order.

1   22.   The medium of claim 19 in which the functions switch

2   periodically and concurrently between the first and second

3   directions.

1   23.   An apparatus implementing a two-dimensional inverse

2   discrete cosine transform, comprising:

3   two one-dimensional inverse discrete cosine transform

4   blocks;

5   a memory block;

6   a sequencer block, the sequencer block alternately being

7   in one of two states, each state indicating the direction each

8   one-dimensional inverse discrete cosine transform block

9   operates in; and

10   an address generator block.
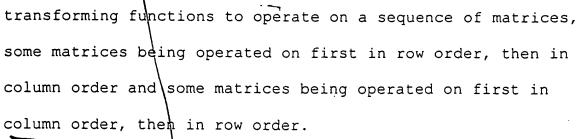
1   24.   The apparatus of claim 23 in which the address

2   generator block is to generate addresses for the one-

3   dimensional inverse discrete cosine transform blocks in the

4   direction indicated by the state of the sequencer.

1   25.   A computer system including a processor, comprising:

2   two one-dimensional inverse discrete cosine transform

3   blocks;

4   a memory block;

5   a sequencer block, the sequencer block alternately being

6   in one of two states, each state indicating the direction each

7   one-dimensional inverse discrete cosine transform block

8   operates in; and

9   an address generator block.

1   26.   The system of claim 25 in which the address

2   generator block is to generate addresses for the one-

3   dimensional inverse discrete cosine transform blocks in the

4   direction indicated by the state of the sequencer.

1   27.   A method of implementing a two-dimensional inverse

2   discrete cosine transform, comprising:

3   executing two one-dimensional inverse discrete cosine

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4   transforming functions to operate on a sequence of matrices,

5   some matrices being operated on first in row order, then in

6   column order and some matrices being operated on first in

7   column order, then in row order.